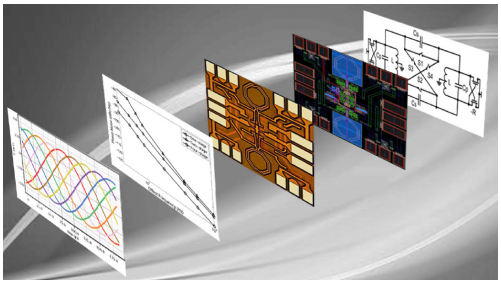
A text book on

Analog Circuits



Useful for IAS, IES, GATE, PSUs and other competitive examinations

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Dedicated to

My Wife

A. Smitha

who believes, in

The best teacher teaches from the heart,
…. not from the book….

PREFACE

I have great pleasure in writing the book of core subject of Electronics Engineering viz. **Analog Circuits.** A thorough understanding of the concepts developed in this book will prepare the reader for more advanced course on the subject. The entire syllabus of Analog circuits is presented in a simple and lucid style to make it comprehensible to an average student. This text book has been written to meet the requirements for the students of B.E./B.Tech., ECE, EEE, EIE.

In this book, I have tried to present the approach for competitive examinations like GATE, IES and IAS. While teaching various categories of students, I understood that, it becomes very easy for the students when things are explained by going through the fundamentals. So in the present book, I tried to explain most of the topics through the basics. The ***Questions with Solutions*** which already appeared in competitive examinations like GATE, IES are incorporated in each chapter.

First, I would like to thank **Mr. B. Singh** (Chief Managing Director, MADE EASY Group) for giving me the opportunity for writing the text book. His constructive suggestions and support helped me a lot.

I express my heartfelt regard and gratitude to my teacher Dr. Srinivas Rao from whom I have learnt the subject matter and which gave me inspiration to write this book.

I would also like to thank my H.O.D. Dr. Koteswara Rao and Principal Dr. Chinna Keshava Rao (CBIT), Mr. Sudarshan Reddy (Associate Prof. in CBIT) who always inspire me in discipline and hard work.

A special thanks to Mr. Sai Prasad who always, encourages me and gave me the first opportunity to teach for competitive exams.

I express my sincere gratitude to my favorite Sir, Mr. Prem R. Chadha, friends M.V. Kiran Kumar, Ramana Reddy, Krishna Kumar, Jagan, Krishna who always direct me in a right path.

Last but not the least, I also thank MADE EASY staff especially Vinod Kumar and Md. Asim who put their sincere efforts to develop this book in time.

Any comments and suggestions for the improvement of this book will be thankfully acknowledged and incorporated in the next edition.

A. Rajkumar

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■■■■

CHAPTER 1

BJT BIASING & THERMAL STABILIZATION

About This Chapter

- Operating point and DC load line.
- AC load line.
- Stability factors S, S′ and S″.
- Various biasing circuits like fixed bias, collector to base bias and self bias.
- Compensation circuits.
- Thermal run-away and conditions to maintain thermal stability.

1 BJT Biasing & Thermal Stabilization

1.1 Operating Point and DC Load Line

- It is clear that the transistor functions most linearly when it is constrained to operate in its active region.
- To establish an operating point in this region it is necessary to provide appropriate direct potentials and currents, using external sources.
- Once an operating point Q is established as shown below:

ANALYSIS

Assume common emitter amplifier circuit

In DC analysis,

(i) ac should be grounded

(ii) $X_c \propto \frac{1}{f}$, as $f \to 0$, $X_c \to \infty$

$\therefore$ Capacitor is open.

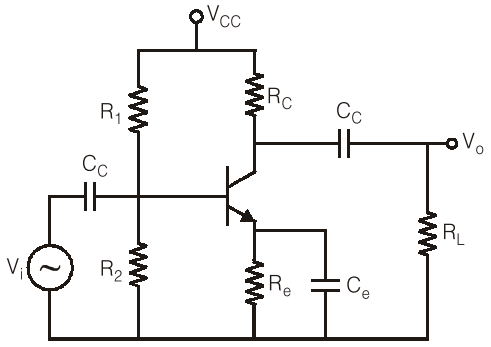


Figure 1.1 Common emitter amplifier

DC Equivalent Model

The output loop equation is given by

$$V_{CC} = I_C(R_C + R_e) + V_{CE}$$

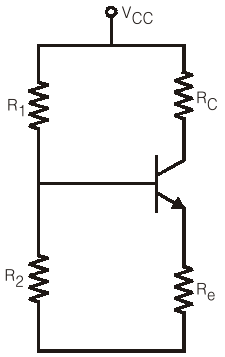
$$I_C = \frac{V_{CC}}{R_C + R_e} - \frac{V_{CE}}{R_C + R_e}$$

Above equation represents like a straight line y = mx + C

When $I_C = 0, \quad (V_{CE})_{max} = V_{CC}$

$$V_{CE} = 0, \quad (I_C)_{max} = \frac{V_{CC}}{R_C + R_e}$$

$$\text{Slope of DC load line} = -\frac{1}{R_C + R_e}$$



Output Characteristics of Common Emitter

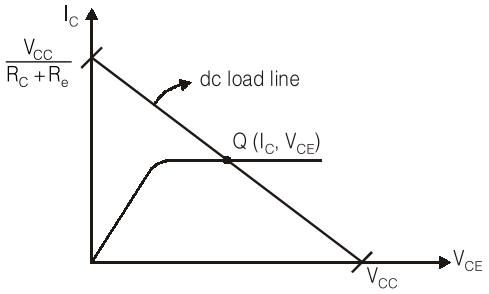


Fig. 1.2 DC load line and Q point

Q Point

"The intersection point between the dc load line and sample graph of I_C is called as operating point (or) Quiescent point".

DC Load Line

"The locus of all the Q points are concentrated on a line called as DC load line".

- When time varying excursions of the input signal (base current, for example) is applied to common emitter amplifier, should cause an output signal (collector voltage or collector current) of the same wave form.
- If the output signal is not a faithful reproduction of the input signal, for example, if it is clipped on one side. The operating point is unsatisfactory and should be relocated on the collector characteristics.
- The question now naturally arises as, how to choose the operating point.
- Note that even if we are free to choose R_c, R_L, R_b and V_{CC}, we may not operate the transistor every where in the active region, because the various transistor ratings limit the range of useful operation.
- These ratings are

  (i) $(V_{CE})_{max}$ **(ii)** $(I_C)_{max}$ **(iii)** $P_{c\,max}$

Capacitive Coupling

- The capacitor C_{b1} is to couple the input signal to the transistor, as indicated in the Figure (1.3).
- In this diagram, one end of V_i is at ground potential, and the collector supply V_{CC} also provides the biasing base current I_B.
- Under quiescent conditions (no input signal), C_{b1} (called a blocking capacitor) acts as an open circuit because the reactance of a capacitor is infinite at zero frequency (dc).

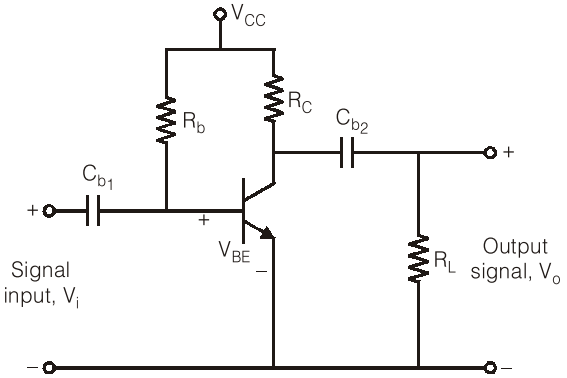


Figure 1.3 Fixed bias circuit

- The capacitances C_{b1} and C_{b2} are chosen large enough so that, at the lowest frequency of excitation their reactances are small enough so that they can be considered to be short circuits.
- These coupling capacitors block dc voltages but freely pass signal voltages.

  For example, the quiescent collector voltage does not appear at the output, but V_o is an amplified replica of the input signal V_i.
- The ac output signal voltage may be applied to the input of another amplifier with out affecting its bias, because of the blocking capacitor C_{b2}.

DC and AC Load Lines

- We noted that under dc conditions C_{b2} acts as an open circuit. Hence the quiescent collector current and voltage are obtained by drawing a static (dc) load line.
- If $R_L = \infty$ and if the input signal (base current) is large and symmetrical, we must locate the operating point Q_1 at the centre of the DC load line. In this way the collector voltage and current may vary approximately symmetrically around the quiescent values V_C and I_C respectively.

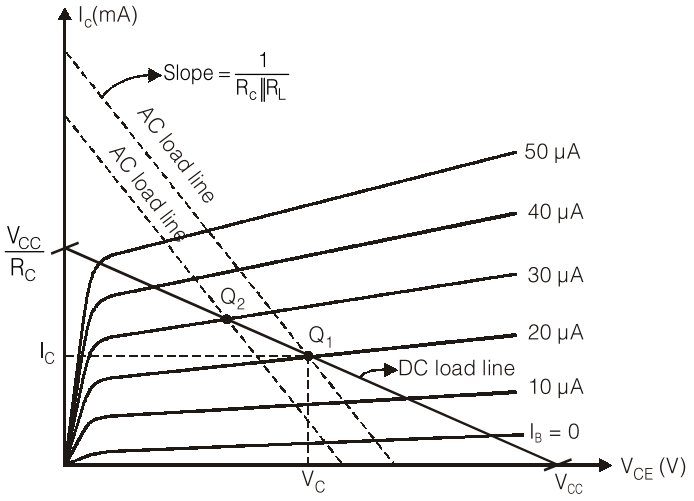
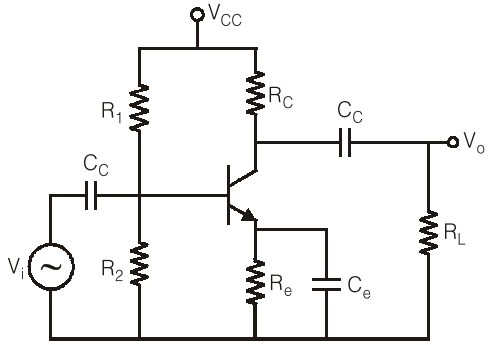


Figure 1.4 DC and AC load line

- If $R_L \neq \infty$, however, a dynamic (ac) load line must be drawn.
- Since, we have assumed that, at the signal frequency, C_{b2} acts as a short circuit, the effective load R_L' at the collector is R_C in parallel with R_L.

AC Load Line Analysis

Assume CE amplifier circuit:



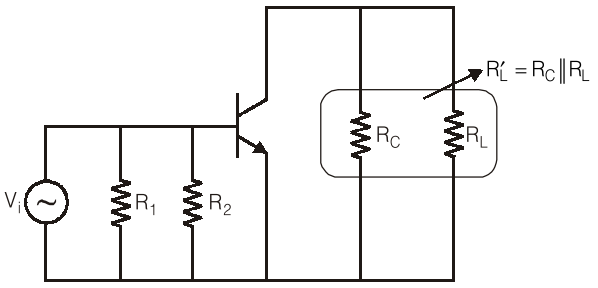
AC Analysis

(i) DC should be grounded.

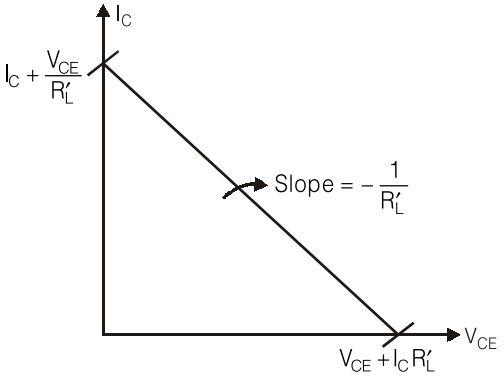
(ii) $X_C \propto \frac{1}{f}$, as $f \to \infty \therefore X_c \to 0$

i.e. capacitor acts as short circuit.

AC Equivalent Model



AC Load Line



$$\text{Slope of ac load line is } -\frac{1}{R'_L} = -\frac{1}{R_C \| R_L}$$

- We observe that the input signal may swing a maximum of approximately 20 μA around Q_1 because, if the base current decreases by more than 20 μA, the transistor is driven off.
- If a larger input swing is available, then in order to avoid cut-off during a part of the cycle. The quiescent point must be located at a higher current.
- Suppose we locate Q_2 on the dc load line such that a line with a slope corresponding to the ac resistance R'_L and drawn through Q_2 gives as large as output as possible with out too much distortion.
- The choice of Q_2 allows an input peak current swing of about 30 μA.

1.2 Temperature Dependence on Transistor Parameters

The sources of instability of I_C are essentially three:

(i) Reverse saturation current I_{CO}

(ii) Base-emitter voltage V_{BE}

(iii) Current gain β

- **I_{CO} Versus Temperature**

  "I_{CO} increases by 7%/°C rise in temperature".

  (or)

  "I_{CO} doubles for every 10°C rise in temperature".

  i.e. as temperature increases, I_{CO} also increases.

- **V_{BE} Versus Temperature**

  "The base to emitter voltage V_{BE}, which decreases at the rate of 2.5 mV/°C for both Ge and Si transistors."

  $$\frac{dV_{BE}}{dT} = -2.5 \text{ mV/°C}$$

  i.e. as temperature increases, V_{BE} decreases.

- **β Versus Temperature**

  (a) β increases with temperature

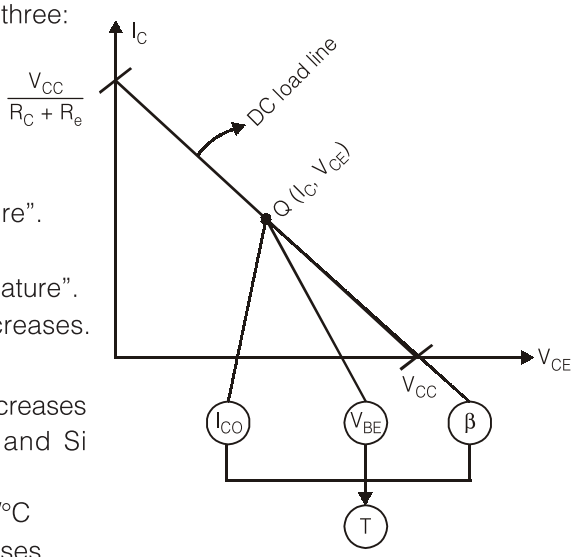


Figure 1.5 DC load line and Q point

(b) Replacement of Transistor

- We see that the spacing of the output characteristics will increase or decrease as β increases or decreases.
- Though transistors are identified by a type number, but even for a given type, the characteristics differ from piece to piece.
- β is the ratio of collector current I_C and base current I_b. As for the same base current, the collector current of the transistor will vary from replacement of the device.
- Generally β is greater for the replacement of transistor.

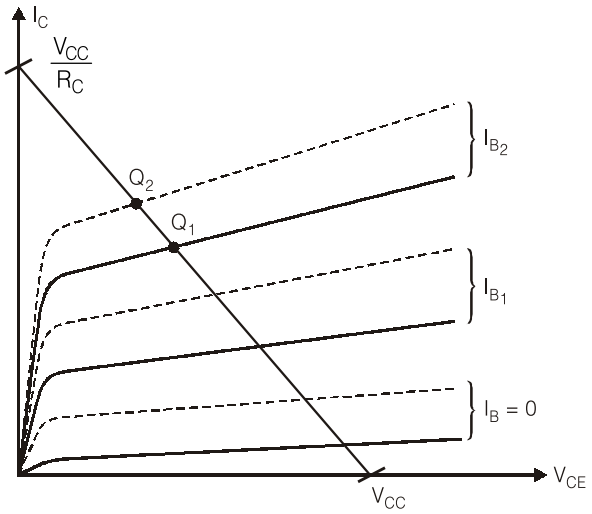


Figure 1.6 Common emitter characteristics

1.3 Stability Factor

"It is a measure of variation in the operating point with respect to the temperature is called as stability factor".

I_C is a function of I_{CO}, V_{BE} and β. It is convenient to introduce the three partial derivatives of I_C with respect to these variables. These derivatives are called the stability factors S, S′ and S″.

$$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}}$$

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$$

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$$

Expression for Stability Factor

$$I_C = \beta I_b + (1+\beta) I_{CO} \quad \text{d.w.r.t } I_C$$

$$1 = \beta \frac{\partial I_b}{\partial I_c} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\boxed{S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\dfrac{\partial I_b}{\partial I_c}}}$$

Conclusion:

- Ideally the stability factor should be zero.
- Practically stability factor should be very very less.

$$P_C = V_{cc} I_c - I_c^2 (R_c + R_e)$$

Taking derivative w.r.t. I_C

$$\frac{\partial P_c}{\partial I_c} = V_{cc} - 2I_c (R_c + R_e)$$

Stability factor S,

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{\partial I_C}{\partial T_j} \times \frac{\partial T_j}{\partial I_{CO}}$$

We know that I_{co} increases at the rate of 7% per°C

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07\, I_{CO}$$

or
$$\frac{\partial T_j}{\partial I_{CO}} = \frac{1}{0.07\, I_{CO}}$$

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07\, I_{CO}$$

$$\boxed{\left\{V_{CC} - 2I_C (R_C + R_e)\right\} \times S \times 0.07 I_{CO} < \frac{1}{\theta}}$$

Conclusion

The following three conditions leads to thermal run-away:

(i) $\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$

(ii) $\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$

(ii) $\left\{V_{CC} - 2I_C (R_C + R_e)\right\} \times S \times 0.07 I_{CO} < \frac{1}{\theta}$

SUMMARY

- The collector current of a transistor varies with I_{CO}, β and V_{BE} which in turn are dependent on temperature variation.
- Stability factor S is given by

$$S = \frac{\partial I_c}{\partial I_{co}} = \frac{1+\beta}{1-\beta \frac{\partial I_b}{\partial I_c}}$$

- Fixed bias circuit is the simplest biasing arrangement and has a stability factor S = 1 + β.
- Collector to base bias circuit is an improvement over fixed bias circuit and has a stability factor

$$S = \frac{1+\beta}{1+\beta \frac{R_c}{R_b + R_c}}$$

- The self bias circuit consists of three resistors R_1, R_2, R_e, usually. The R_E is bypassed with a large value capacitor C_E. The stability factor,

$$S = \frac{1+\beta}{1+\beta\dfrac{R_e}{R_b+R_e}}$$

for obtaining low value of S, it is necessary to choose a low value of $\frac{R_b}{R_e}$.

- Bias compensation can be achieved either by use of diode, thermistor or sensistor.
- Stability factor $S' = \frac{\partial I_C}{\partial V_{BE}}$ and stability factor $S'' = \frac{\partial I_C}{\partial \beta}$ can both be reduced if stability factor S is reduced.
- Condition for thermal stability or avoiding thermal runaway are

$$\Rightarrow \quad \frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad \text{(or)} \quad \frac{\partial P_c}{\partial T_j} < \frac{1}{\theta} \quad \text{(or)} \quad [V_{CC} - 2I_C(R_c + R_e)] \times S \times 0.07 I_{CO} < \frac{1}{\theta}$$

where θ = thermal resistance.

- Best possible of choosing the operating point is $V_{CE} = \frac{V_{cc}}{2}$.

GATE AND IES QUESTIONS

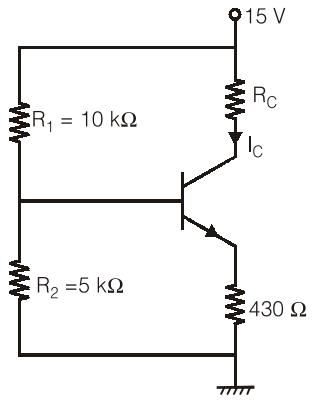
Q.1 Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in

(a) only the temperature
(b) only the β
(c) Both temperature and β
(d) none

Exp. (c)

R_e resistor works as a negative feedback which gives stability of the circuit. Therefore it stabilizes against the variation of both temperature and β.

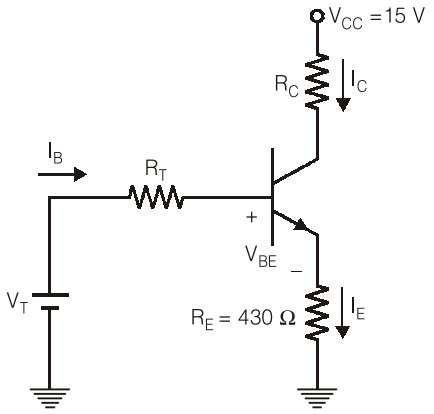
Q.2 In the circuit of the figure, assume that the transistor is in the active region. It has a large β and its base-emitter voltage is 0.7 V. The value of I_c is



(a) Indeterminate since R_c is not given
(b) 1 mA
(c) 5 mA
(d) 10 mA

Exp. (d)

The Thevenin equivalent is shown below:



$$V_T = \frac{R_2}{R_1 + R_2} V_{cc}$$

$$= \frac{5}{10+5} \times 15 = 5 \text{ V}$$

Since β is large

$$I_C \approx I_E,\ I_B \approx 0 \text{ and}$$

$$I_E = \frac{V_T - V_{BE}}{R_E}$$

$$= \frac{5 - 0.7}{0.430\,\text{k}\Omega} = \frac{4.3}{0.430\,\text{k}\Omega} = 10\,\text{mA}$$

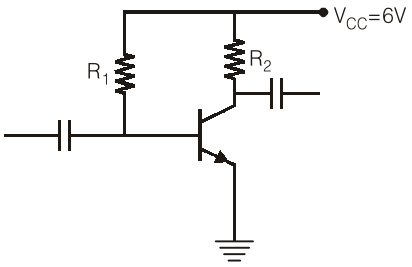
Q.3 In the amplifier circuit shown in the figure, the values of R_1 and R_2 are such that the transistor is operating at V_{CE} = 3 V and I_C = 1.5 mA, when its β is 150. For a transistor with β of 200, the operating point (V_{CE}, I_C) is

(a) (2 V, 2 mA)

(b) (3 V, 2 mA)

(c) (4 V, 2 mA)

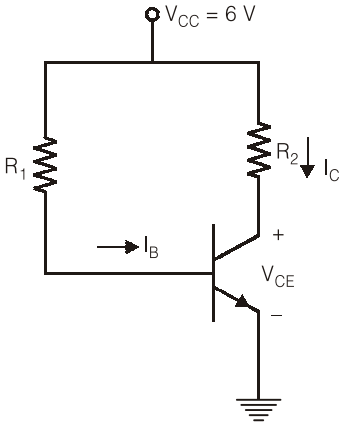
(d) (4 V, 1 mA)



Exp. (a)

The DC equivalent circuit is shown below:

First case:



$$V_{CC} - I_{C_1} R_2 - V_{CE_1} = 0$$

$$6 - 1.5\text{ mA}\ R_2 - 3 = 0$$

$$R_2 = 2\ \text{k}\Omega$$

$$I_{B_1} = \frac{I_{C_1}}{\beta_1} = \frac{1.5\,\text{mA}}{150} = 0.01\,\text{mA}$$

Second case:

I_{B_2} will be equal to I_{B_1} as there is no change in R_1

$$I_{C_2} = \beta_2 I_{B_2} = 200 \times 0.01\text{ mA} = 2\text{ mA}$$

$$V_{CE_2} = V_{CC} - I_{C_2} R_2 = 6 - 2\text{ mA} \times 2\text{ k}\Omega$$

$$= 2\text{ V}$$

Exp. (d)

For the transistor to be in saturation

$$I_B > \frac{I_C}{\beta}$$

Q.31 If for a silicon n-p-n transistor, the base-to-emitter voltage (V_{BE}) is 0.7 V and the collector to base voltage (V_{CB}) is 0.2 V, then the transistor is operating in the

(a) normal active mode (b) saturation mode

(c) inverse active mode (d) cutoff mode

Exp. (a)

$$V_{CE} = V_{BE} + V_{CB}$$
$$= 0.7 + 0.2$$
$$= 0.9 \text{ V}$$
$$(V_{CE})_{sat} = 0.2 \text{ V}$$

Therefore $V_{CE} > (V_{CE})_{sat}$

It is in normal active mode

REVIEW QUESTIONS

1. What is the purpose of biasing a transistor? Indicate the methods of biasing and compare them.
2. Define the three different stability factors and give an expression that determine the variation of collector current in terms of stability factor.
3. Explain the effect of temperature on various parameters of a transistor amplifier circuit and discuss the methods of stabilization of the operating point.
4. Draw a fixed bias circuit and explain its drawbacks in detail.
5. Derive expressions for stability factors of a self bias circuit.
6. Explain how stability is improved in a self bias circuit.
7. Give a transistor circuit that employs a thermistor to compensate the variation of parameters with temperature and explain the circuit operation.
8. What is a sensistor? Explain how it can be employed in a transistor circuit to compensate the variation of operating point with temperature.
9. Distinguish between stabilization and compensation techniques. Discuss about compensation techniques in detail.
10. What do you understand by thermal run away? Derive the condition for avoiding thermal run-away in a transistor. Explain the term thermal resistance and derive the condition for thermal stability of BJT.

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